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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,580	07/29/2003	Hiroyuki Abe	108066-00092	4127

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/628,580	ABE ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 12-15* is/are rejected.

7)☒ Claim(s) *11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-7, 10 and 12-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Clark et al. (USP 6664775).

As to claim 1, Clark et al. discloses in figure 1 a semiconductor integrated circuit comprising: an internal supply voltage generation circuit (40) which generates an internal supply voltage (VDD) by decreasing an external supply voltage (VBATTERY; column 3, lines 39-41); and an internal circuit (circuit, not shown, in circuit 50) which operates with the internal supply voltage supplied thereto, wherein the internal supply voltage generation circuit changes the internal supply voltage level to be generated in accordance with an operation speed of the internal circuit (column 3, lines 55-60).

As to claim 2, figure 1 and column 3, lines 55-60, a clock control circuit (30) which generates an internal clock signal (CLOCK) having a frequency controlled in accordance with the operation speed of the internal circuit, wherein, when the internal clock signal is controlled to have a first frequency, the internal supply voltage is controlled to have a first voltage, and when the internal clock signal is controlled to have a second frequency which is lower than the first

frequency, the internal supply voltage is controlled to have a second voltage which is lower than the first voltage.

As to claim 3, figure 1 and column 3, lines 55-60, disclose a clock and voltage control circuit (30, 50) which generates an internal clock signal (CLOCK) having a frequency controlled in accordance with the operation speed of the internal circuit, the clock and voltage control circuit controls the internal clock signal frequency, and also controls the internal supply voltage level generated by the internal supply voltage generation circuit to become a level corresponding to the internal clock signal frequency.

As to claim 4, figure 1 and column 3, lines 55-60, disclose the internal clock signal is controlled to have a first frequency, the internal supply voltage is controlled to have a first voltage, and when the internal clock signal is controlled to have a second frequency which is lower than the first frequency, the internal supply voltage is controlled to have a second voltage which is lower than the first voltage.

As to claims 5-7, it is inherent that the internal supply voltage is set higher than the minimum voltage level, over which the internal circuit is operational at each internal clock signal frequency.

As to claim 10, figure 5 shows that no supply voltage is generated in the standby mode. Therefore, it is inherent that when the internal circuit is controlled to set into standby mode, the internal supply voltage generation circuit suspends generation of the internal supply voltage.

As to claim 12, it is inherent that when turning on power, the internal supply voltage is controlled to have a maximum internal supply voltage level.

As to claim 13, figure 1 shows that in accordance with a program executed by a

CPU (50) in the internal circuit, the internal clock signal frequency generated by the clock control circuit is controlled, and further the internal supply voltage level generated by the internal supply voltage generation circuit is controlled.

As to claim 14, column 3, lines 55-60, discloses the executed program determines an operation is performed in either a high-speed operation mode or a low-speed operation mode, and when determined as being in the high-speed operation mode, the internal clock signal frequency is controlled to be higher, and also the internal supply voltage is controlled to be higher, while when in the low-speed operation mode, the internal clock signal frequency is controlled to be lower, and also the inter supply voltage is controlled to be lower.

3. Claims 1-9 and 12-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Clark et al. (USP 6425086).

As to claim 1, Clark et al. discloses in figure 1 a semiconductor integrated circuit comprising: an internal supply voltage generation circuit (120) which generates an internal supply voltage (VDD) by decreasing an external supply voltage (VBATTERY); and an internal circuit (circuit, not shown, in circuit 110) which operates with the internal supply voltage supplied thereto, wherein the internal supply voltage generation circuit changes the internal supply voltage level to be generated in accordance with an operation speed of the internal circuit (column 7, lines 1-14).

As to claim 2, figure 1 and column 7, lines 1-14, a clock control circuit (circuit, not shown in 110) which generates an internal clock signal having a frequency controlled in accordance with the operation speed of the internal circuit, wherein, when the internal clock signal is controlled to have a first frequency, the internal supply voltage is controlled to have a

first voltage, and when the internal clock signal is controlled to have a second frequency which is lower than the first frequency, the internal supply voltage is controlled to have a second voltage which is lower than the first voltage.

As to claim 3, figure 1 and column 7, lines 1-14, disclose a clock and voltage control circuit (110) which generates an internal clock signal having a frequency controlled in accordance with the operation speed of the internal circuit, the clock and voltage control circuit controls the internal clock signal frequency, and also controls the internal supply voltage level generated by the internal supply voltage generation circuit to become a level corresponding to the internal clock signal frequency.

As to claim 4, figure 1 and column 7, lines 1-14, disclose the internal clock signal is controlled to have a first frequency, the internal supply voltage is controlled to have a first voltage, and when the internal clock signal is controlled to have a second frequency which is lower than the first frequency, the internal supply voltage is controlled to have a second voltage which is lower than the first voltage.

As to claims 5-7, it is inherent that the internal supply voltage is set higher than the minimum voltage level, over which the internal circuit is operational at each internal clock signal frequency.

As to claims 8 and 9, figure 6 shows that when the internal supply voltage is controlled to increase from the second voltage to the first voltage, the internal clock signal frequency is controlled to change from the second frequency to the first frequency after increasing the internal supply voltage generated by the internal supply voltage generation circuit to the first voltage is ascertained to complete.

As to claim 12, it is inherent that when turning on power, the internal supply voltage is controlled to have a maximum internal supply voltage level.

As to claim 13, figure 1 shows that in accordance with a program executed by a CPU (110) in the internal circuit, the internal clock signal frequency generated by the clock control circuit is controlled, and further the internal supply voltage level generated by the internal supply voltage generation circuit is controlled.

As to claim 14, column 7, lines 1-14, discloses the executed program determines an operation is performed in either a high-speed operation mode or a low-speed operation mode, and when determined as being in the high-speed operation mode, the internal clock signal frequency is controlled to be higher, and also the internal supply voltage is controlled to be higher, while when in the low-speed operation mode, the internal clock signal frequency is controlled to be lower, and also the inter supply voltage is controlled to be lower.

As to claim 15, figure 1 shows a first register (125) which supplies a voltage control signal to the internal supply voltage generation circuit; and a second register (112) which supplies an operation mode signal to the clock control circuit, wherein the CPU (110) modifies data stored in at least either one of the first register and the second register, depending on the executed program.

Allowable Subject Matter

4. Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 11 would be allowable because the prior art fails to teach or suggest an external reset circuit which generates an initialization signal to restore the internal circuit from the standby mode, wherein, in response to said initialization signal, the internal supply voltage generation circuit resumes generation of the internal supply voltage.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Quan Tra
Patent Examiner

September 20, 2004